11-24-00

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**Practitioner's Docket No. RPS920000100US1**
**Customer No. 25299**

**PATENT**



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Box Patent Application**
**Assistant Commissioner for Patents**
**Washington, D.C. 20231**

## NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): R. M. Clemo et al;

For (title): **FAIL SAFE CIRCUIT WITH RESET CAPABILITY FOR A POWER SUPPLY**



### 1. Type of Application

This transmittal is for an original (nonprovisional) application.

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**CERTIFICATION UNDER 37 C.F.R. sections 1.8(a) and 1.10***
*(When using Express Mail, the Express Mail label number is **mandatory**;*
*Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

**MAILING**

☒ deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

**37 C.F.R. section 1.8(a)**

☐ with sufficient postage as first class mail.

**37 C.F.R. section 1.10***

☒ as "Express Mail Post Office to Address" Mailing Label No. EJ207756259US (**mandatory**)

**TRANSMISSION**

☐ transmitted by facsimile to the Patent and Trademark Office.

Date: Nov. 22, 2000

Amirah Scarborough
**Signature**

Amirah Scarborough
(*type or print name of person certifying*)

2. **Papers Enclosed**

A. Required for filing date under 37 C.F.R. 1.53(b) (Regular) or 37 C.F.R. 1.153 (Design) Application

5 Page(s) of Specification
5 Page(s) of Claims
2 Sheet(s) of Drawing(s)--Informal
3 Page(s) of declaration and power of attorney
1 Page(s) of abstract

3. **Assignment**

An assignment of the invention to International Business Machines Corporation is attached. A separate "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" is also attached.

4. **Fee Calculation (37 C.F.R. section 1.16)**

Regular Application

CLAIMS AS FILED

| Claims | Number Filed | Basic Fee Allowance | Number Extra | Rate | Basic Fee 37 CFR 1.16(a) $710.00 |
|---|---|---|---|---|---|
| Total Claims (37 CFR 1.16(c)) | 26 | - 20 = | 6 x | $18.00 | $108.00 |
| Independent Claims (37 CFR 1.16(b)) | 3 | - 3 = | 0 x | $80.00 | $0.00 |
| Multiple Dependent Claim(s), if any (37 CFR 1.16(d)) | | | + | $260.00 | $0.00 |
| Filing Fee Calculation | | | | | $818.00 |

**5. Fee Payment Being Made at This Time**

| | |
|---|---|
| Enclosed | |
| Filing Fee | $818.00 |
| Recording assignment ($40; 37 C.F.R. section 1.21(h)) (See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) | $40.00 |
| **Total Fees Enclosed** | $858.000 |

**6. Method of Payment of Fees**

Charge Account No. 09-1990 in the amount of $858.00.
A duplicate of this transmittal is attached.

**7. Authorization to Charge Additional Fees**

The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 09-1990.

37 C.F.R. section 1.16(a), (f) or (g) (filing fees)

**8. Instructions as to Overpayment**
Credit Account No. 09-1990.

Date: 11-22-00

Martin J McKinley
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P. O. Box 12195
Research Triangle Park, NC 27709
919-254-2578
Customer No. 25299

I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231

Signature

**DATE OF DEPOSIT:** Nov. 22, 2000

**EXPRESS MAIL LABEL NO.:** EJ207756259US

**Inventors: Ray M. Clemo; William Hemena; Eino A. Lindfors; and Randhir S. Malik**

# FAIL SAFE CIRCUIT WITH RESET CAPABILITY FOR A POWER SUPPLY

## FIELD OF THE INVENTION

The present invention relates to power supplies, and more particularly to providing a fail safe monitoring circuit with reset capability for a power supply.

## BACKGROUND OF THE INVENTION

While the size and speed of electronic components have received much focus and attention in the advancement of digital technology, ensuring proper power delivery to the components has remained a concern. The various branches within a system that rely on a power supply tend to be numerous and require differing levels of power. As the number of components within a system increases, the chance for failures and damage of the power supply of a system also increases.

Circuits to shutdown a power supply once a preset limit has been exceeded are usually not fail safe. For example, if any component within a monitoring circuit for a power supply fails, the protection provided by the circuit is lost. Furthermore, there is no built-in ability to detect and correct failures that are temporary within the monitoring circuit.

Accordingly, a need exists for a technique that provides a fail safe monitoring circuit for a power supply that protects against short circuit and overload conditions while also providing recovery from temporary fault conditions to reset the fail safe circuit and resume normal operations. The present invention addresses such a need.

## SUMMARY OF THE INVENTION

The present invention provides aspects of a fail safe circuit for protecting power supply operation from a failure. The fail safe circuit shutdowns at least one power supply when a preset threshold is exceeded and resets to resume normal operation following a temporary fault condition. The fail safe circuit includes a switch coupled to a voltage signal line of a branch of a power supply system, a current sense resistor coupled to the switch for detecting a failure condition in the branch, and a latch coupled to the current sense resistor and the switch for turning the switch off during the failure condition.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an overall block diagram of a system that includes a fail safe circuit in accordance with the present invention.

Figure 2 illustrates a fail safe circuit in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to a fail safe circuit with reset capability for a power supply. The following description is presented to enable one of ordinary skill in the art to

make and use the invention and is provided in the context of a patent application and its requirements. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

Figure 1 illustrates a block diagram of a system in accordance with the present invention that includes a fail safe circuit and portions of a typical computer processing system, such as a computer server or the like. As represented by Figure 1, coupled to a power backplane 10 of a system 12 is a processing system board 14 and at least one power supply 16. The system board 14 is coupled to a host of input and output devices (not shown), e.g., a keyboard, a pointing device, a flexible disk drive, and a monitor. Power, perhaps at multiple direct current voltage levels (if necessary), are applied by the power supply 16 to the power backplane 10. This applied power is distributed by the power backplane 10 via connections to the system I/O board as well as to other components (such as other backplanes and devices), not shown, of the system 12 which are mounted or connected to the power backplane. Thus, there can be several branches of the system that extend from the power supply 16 via the backplane 10. In accordance with the present invention, the power backplane 10 includes a fail safe circuit 20 for each branch, which is described in more detail with reference to Figure 2.

In general, the fail safe circuit 20 operates to determine if current flowing through a branch exceeds a preset threshold, e.g., a 240 VA (volt-ampere) power limit, and to reset operation once a temporary fault is cleared. The fail safe circuit 20 shown in Figure 2 includes a transistor switch 22 coupled to a voltage signal line, VIN, for the branch, and

which is kept on during normal operation of the power system. Resistor 24 (e.g., 5 milliohm) coupled to the transistor 22 functions as a current sense resistor to monitor the branch current. Once the branch current exceeds a safe current, e.g., causes the preset threshold of 240 VA to be exceeded for the branch, the corresponding voltage level across the resistor 24 is sensed by comparator 25 and output to a comparator 26, which outputs a HIGH level signal. In turn, the output HIGH signal from comparator 26 sets latch 28. With the latch 28 set, the transistor switch 22 is turned off, thereby protecting the branch.

In order to protect against an internal fault which causes transistor switch 22 to short, combination logic 30 (e.g., an AND gate) is employed. When transistor switch 22 shorts out, the output voltage, VOUT, will be HIGH and the preset threshold/240 VA limit will be exceeded. Combinational logic 30 senses the HIGH level of VOUT and combines that with the level of the output signal from comparator 26. Since the output of comparator 26 will be HIGH due to the preset threshold being exceeded, combinational logic 30 outputs a HIGH level signal as a Shutdown Signal to shutdown the whole power system 16.

At times, a temporary fault causes a shutdown of the branch or whole system. For such momentary fault conditions, it is quite possible that the fault has been cleared and there is no overload fault condition or short circuit condition anymore. To account for this possibility, a current source 32 is included in the fail safe circuit 20 to feed a fixed current. By way of example, a current source providing 0.1 amp current would be suitable for a circuit monitoring for a 240 VA threshold. If the voltage measured at VOUT is found to be higher than a reference voltage (VREF2), e.g., 0.6 volt for a twelve-volt output, by a comparator 34, the output of the comparator 34 goes HIGH. The HIGH level signal acts as a

RESET signal for the latch 28. Thus, once the temporary fault is cleared with the latch 28 reset, the transistor switch 22 is turned on, and normal operation resumes.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. For example, it should be appreciated that the values associated with the various components of the fail safe circuit shown in Figure 2 can be chosen as necessary for particular system requirements. Thus, while the description has provided values suitable for use when monitoring for a 240 VA threshold, other values may be appropriate for other threshold levels, as is well understood by those skilled in the art. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

## CLAIMS

What is claimed is:

1. A system for protecting power supply operation from a failure, the system comprising:

at least one power supply; and

a power backplane coupled to the at least one power supply, wherein the power backplane includes a fail safe circuit that shutdowns the at least one power supply when a preset threshold is exceeded and resets to resume normal operation following a temporary fault condition.

2. The system of claim 1 wherein the preset threshold corresponds to 240 VA power level.

3. The system of claim 1 wherein the fail safe circuit further comprises:

a switch coupled to a voltage signal line of a branch of a power supply system;

a current sense resistor coupled to the switch for detecting a failure condition in the branch; and

a latch coupled to the current sense resistor and the switch for turning the switch off during the failure condition.

4. The system of claim 3 wherein the fail safe circuit further comprises at least one comparator coupled between the current sense resistor and the latch to set the latch during the failure condition.

5. The system of claim 4 wherein the fail safe circuit further comprises combinational logic coupled to the at least one comparator and the current sense resistor for outputting a shutdown signal when the switch is shorted.

6. The system of claim 5 wherein the combinational logic further comprises an AND gate.

7. The system of claim 5 wherein the fail safe circuit further comprises a current source coupled to the voltage signal line to supply a current between an input node and an output node of the fail safe circuit.

8. The system of claim 7 wherein the fail safe circuit further comprises a reset comparator coupled to the output node for providing a signal level to reset the latch.

9. The system of claim 8 wherein the reset latch turns the switch on for resumption of normal circuit operation following a temporary short circuit of the switch.

10. A method for protecting power supply operation from a failure, the method comprising the steps of:

(a) providing a fail safe circuit in a power backplane; and

(b) utilizing the fail safe circuit to shutdown at least one power supply when a preset threshold is exceeded and to reset and resume normal operation following a temporary fault.

11. The method of claim 10 wherein providing a fail safe circuit step (a) further comprises the steps of:

(a1) providing a switch coupled to a voltage signal line of a branch of a power supply system;

(a2) providing a current sense resistor coupled to the switch for detecting a failure condition in the branch; and

(a3) providing a latch coupled to the current sense resistor and the switch for turning the switch off during the failure condition.

12. The method of claim 11 further comprising the step of (c) providing at least one comparator coupled between the current sense resistor and the latch to set the latch during the failure condition.

13. The method of claim 12 further comprising the step of (d) providing combinational logic coupled to the at least one comparator and the current sense resistor for outputting a shutdown signal when the switch is shorted.

14. The method of claim 13 wherein the combinational logic further comprises an AND gate.

15. The method of claim 13 further comprising the step of (e) providing a current source coupled to the voltage signal line to supply a fixed current between an input node and an output node of the fail safe circuit.

16. The method of claim 15 further comprising the step of (f) providing a reset comparator coupled to the output node for providing a signal level to reset the latch.

17. The method of claim 16 wherein the reset latch turns the switch on for resumption of normal circuit operation following a temporary short circuit of the switch.

18. The method of claim 10 wherein the preset threshold corresponds to 240 VA power level.

19. A power supply fail safe circuit comprising:

a switch coupled to a voltage signal line of a branch of a power supply system;

a current sense resistor coupled to the switch for detecting a failure condition in the branch; and

a latch coupled to the current sense resistor and the switch for turning the switch off during the failure condition.

20. The circuit of claim 19 wherein the preset threshold corresponds to 240 VA power level.

21. The circuit of claim 19 further comprising at least one comparator coupled between the current sense resistor and the latch to set the latch during the failure condition.

22. The circuit of claim 21 further comprising combinational logic coupled to the at least one comparator and the current sense resistor for outputting a shutdown signal when the switch is shorted.

23. The circuit of claim 22 wherein the combinational logic further comprises an AND gate.

24. The circuit of claim 22 further comprising a current source coupled to the voltage signal line to supply a fixed current between an input node and an output node of the fail safe circuit.

25. The circuit of claim 24 further comprising a reset comparator coupled to the output node for providing a signal level to reset the latch.

26. The circuit of claim 25 wherein the reset latch turns the switch on for resumption of normal circuit operation following a temporary short circuit of the switch.

## ABSTRACT

Aspects of a fail safe circuit for protecting power supply operation from a failure are described. The fail safe circuit shutdowns at least one power supply when a preset threshold is exceeded and resets to resume normal operation following a temporary fault condition. The fail safe circuit includes a switch coupled to a voltage signal line of a branch of a power supply system, a current sense resistor coupled to the switch for detecting a failure condition in the branch, and a latch coupled to the current sense resistor and the switch for turning the switch off during the failure condition.

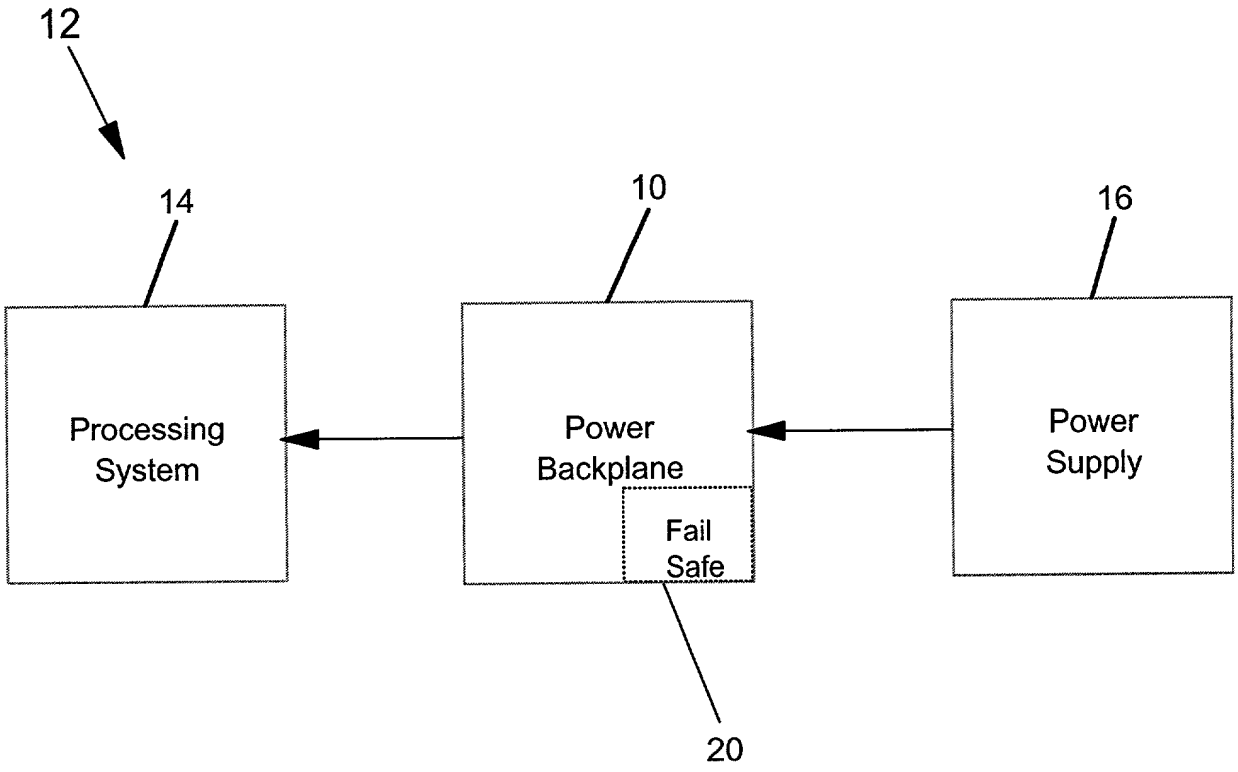
12
14
10
16
Processing System
Power Backplane
Fail Safe
Power Supply
20

FIG. 1

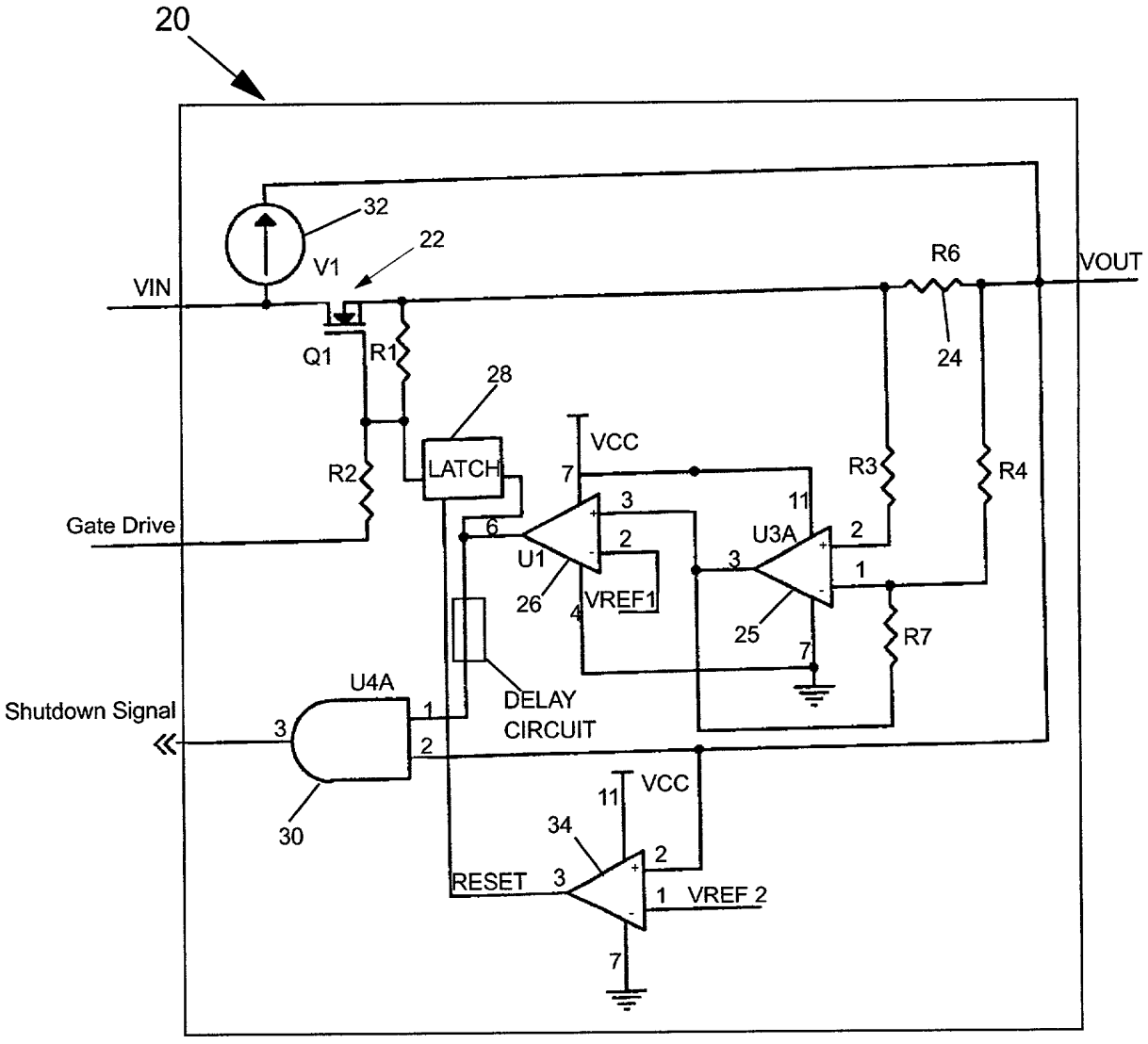
20
32
V1
22
VIN
Q1
R1
R2
28
LATCH
VCC
7
3
6
2
U1
26
VREF1
4
Gate Drive
11
U3A
3
2
1
25
7
R3
R4
R6
VOUT
24
R7
U4A
Shutdown Signal
3
1
2
30
DELAY
CIRCUIT
11
VCC
34
2
RESET
3
1
VREF 2
7

FIG. 2

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

## FAIL SAFE CIRCUIT WITH RESET CAPABILITY FOR A POWER SUPPLY

the specification of which: (check one)

XXX is attached hereto.

_____ was filed on _____
XXX under Attorney's Docket Number RPS920000100US1
_____ as Application Serial No. _____
_____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56.

I hereby claim the benefit of foreign priority under 35 USC 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application the priority of which is claimed:

| Prior Foreign Application(s): | | | Priority Claimed |
|---|---|---|---|
| | | | _____Yes _____No |
| (Number) | (Country) | (Filing Date) | |

I hereby claim the benefit of United States priority under 35 USC 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| | | |
|---|---|---|
| (Application Serial #) | (Filing Date) | (Status) |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

| | | | |
|---|---|---|---|
| **Customer No.** | **25299** | | |
| H. St. Julian | Reg. No. 30,329 | Martin J. McKinley | Reg. No. 31,782 |
| John D. Flynn | Reg. No. 35,137 | Joseph A. Sawyer | Reg. No. 30,081 |
| George Grosser | Reg. No. 25,629 | Janyce R. Mitchell | Reg. No. 40,095 |
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| Doretha L. Robinson | Reg. No. 45,048 | | |

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